Jing (Jane) Li

Curriculum Vitae

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Department of Electrical & Computer Engineering, & Department of Computer Science, University of Wisconsin-Madison
https://wicil.ece.wisc.edu
+1 765-418-5178
jli@ece.wisc.edu

Education

2009	Ph.D.	Electrical & Computer Engineering	Purdue University, West Lafayette, IN, USA
2004	B.Engr.(Hons)	Electrical Engineering	Shanghai Jiao Tong University, Shanghai, China

Positions Held

2017–	**Dugald C.Jackson Assistant Professor**, Department of Electrical & Computer Engineering, University of Wisconsin-Madison, Madison, WI.
2015–2016	**Assistant Professor**, Department of Electrical & Computer Engineering, University of Wisconsin-Madison, Madison, WI.
2013–2014	**Research Staff Member**, Department of Communication and Computation System: Hardware Accelerator and Machine Learning, IBM T. J. Watson Research Center, Yorktown Heights, NY.
2011–2013	**Research Staff Member**, Department of Silicon Technology: Exploratory Nonvolatile Memories, IBM T. J. Watson Research Center, Yorktown Heights, NY.
2010–2011	**Research Staff Member**, Department of Physical Science: Exploratory Nonvolatile Memories, IBM T. J. Watson Research Center, Yorktown Heights, NY.
2009–2010	**Postdoctoral Researcher**, Department of Physical Science: Exploratory Nonvolatile Memories, IBM T. J. Watson Research Center, Yorktown Heights, NY.
Summer, 2008	**Research Intern** (sponsored by IBM PhD Fellowship), Department of Embedded DRAM (eDRAM), IBM Semiconductor Research and Development Center (SRDC), Fishkill, NY.

Honors and Awards

2019	**Best Paper Nominee** [C3], FCCM 2019
2018	Best of CAL (**Best Paper Award** [J1]), IEEE Computer Architecture Letters
2018	Moore Inventor Fellowship Nominee (1 out of 2 university wide), University of Wisconsin-Madison
2018	**NSF CAREER Award**, National Science Foundation
2017	Featured in Madison Magazine (Channel 3000) as a Rising Research Star
2017	Wisconsin Hilldale Faculty Research Fellowship, University of Wisconsin-Madison
2017	**Dugald C. Jackson Faculty Scholar** of Electrical and Computer Engineering (named after the first department chair of ECE), University of Wisconsin-Madison
2016	**DARPA Young Faculty Award**, Defense Advanced Research Projects Agency (one out of 26 nationwide, the first awardee in computer engineering field at UW-Madison)
2016	WARF Innovation Awards (WIA) Finalist, University of Wisconsin-Madison (6 out of 400++ patents)
2014	IBM High Value Patent Application Awards, IBM T. J. Watson Research Center.
2013	**Best Paper Award** ([J12]), VLSI Transactions, IEEE Circuits and Systems Society.
2012	**Outstanding Research Division Technical Achievement Award** (*highest technical award for successfully achieving CEO milestone on Storage Class Memory*), IBM T. J. Watson Research Center.
2010–2015	IBM Invention Achievement Awards, IBM T. J. Watson Research Center.
2009	Best PhD Thesis Award nomination, Purdue University.
2008–2009	IBM PhD Fellowship.
2007	The Dean's and Semester Honors for Outstanding Scholastics Performance, Purdue University.
2005	Magoon Award for Excellence in Teaching, Purdue University.
2004	Meissner Fellowship Award, Electrical and Computer Engineering department, Purdue University

Research Highlights

- Since 2006, I have authored over 100 publications, including conference proceedings, journal articles, patents, etc. on various topics in computer area (ranging from IEDM, IRPS, VLSI Circuit and Technology Symp. to FPGA, FCCM, ASPLOS, CVPR, ICLR, DAC, ICCAD, etc.). A list of these appears on pages 2–8.
- I am one of the 22 PIs in Center for Research on Intelligent Storage and Processing-in-memory (**CRISP**) for SRC Joint University Microelectronics Program (**JUMP**).
- My research greatly benefits from my strong ties with leading technology companies and successful technology transfer experience.
- I have been serving at organizing committee (**first** female conference chair) at International Memory Workshop (*annual meeting with world-wide memory vendors*, *co-organized w/ Intel*, *Micron*, *SK-Hynix*, *CEA-LETI*, *etc.*).
- My research on "*Liquid Silicon*" was reported by media including *Yahoo News*, *Newegg Business*, *Digital Trends*, *inside HPC*, etc..
- My work [C19] on hardware accelerated deep neural network set the **world record** in the best power efficiency and performance density compared to existing FPGA work—including that of industry giants.
- My work [C11] ranked **No.1** on Green Graph 500 list (demonstrated the **most** energy efficient graph analytics system world wide).
- My work [C26] demonstrated the **first** large-scale PCM TCAM chip with heterogeneous monolithic 3D integration, highlighted by Symp. on VLSI Circuits.
- My work [C32] demonstrated the **first** multi-bit PCM chip with heterogeneous monolithic 3D integration to demonstrate a new storage concept of programmable Variable Level Storage (VLC).
- Successfully achieved **CEO milestone** on multi-bit Storage Class Memory at IBM.

Publications

Students under my supervision are denoted by "S"

PhD Thesis

[T1] Jing Li, "Robust and energy-efficient heterogeneous system design in emerging technologies (**nominated for Best Thesis Award**)," Advisor: Prof. Kaushik Roy, PhD thesis, Purdue University, 2009.

Refereed Journal Papers

[J1] Soroosh Khoram^{S}, Yue Zha^{S}, and Jing Li, "An alternative analytical approach to associative processing (**Best of CAL**)," *IEEE Computer Architecture Letters*, **PP**, (99), 1–1, 2018.

[J2] Rohit Shukla, Soroosh Khoram^{S}, Erik Jorgensen, Jing Li, Mikko Lipasti, and Stephen Wright, "Computing generalized matrix inverse on spiking neural substrate," *Frontiers in neuroscience: Neuromorphic engineering*, **12**, 115, Feb. 14, 2018.

[J3] Yue Zha^{S} and Jing Li, "Specialization: A new path towards low power (**invited**)," *ASP Journal of Low Power Electronics*, *2018*, **14**, (2), Feb. 15, 2018.

[J4] Yue Zha^{S} and Jing Li, "CMA: A reconfigurable complex matching accelerator for wire-speed network intrusion detection," *IEEE Computer Architecture Letters*, **PP**, (99), 1–1, 2017.

[J5] Yue Zha^{S} and Jing Li, "IMEC: A fully morphable in-memory computing fabric enabled by resistive crossbar," *IEEE Computer Architecture Letters*, **16**, (2), 123–126, 2017.

[J6] Jing Li, Robert Montoye, Masatoshi Ishii, and Leland Chang, "1 Mb 0.41 μm^2 2T-2R cell nonvolatile TCAM with two-bit encoding and clocked self-referenced sensing (**invited**)," *IEEE Journal of Solid-State Circuits*, **49**, (4), 896–907, 2014.

[J7] K Cil, Y Zhu, Jing Li, CH Lam, and H Silva, "Assisted cubic to hexagonal phase transition in gesbte thin films on silicon nitride," *Thin Solid Films*, **536**, 216–219, 2013.

[J8] Adam Cywar, Jing Li, Chung Lam, and Helena Silva, "The impact of heater-recess and load matching in phase change memory mushroom cells," *Nanotechnology*, **23**, (22), 225201, 2012.

[J9] Xiao Zhang, Jerome Mitard, Lars-Ake Ragnarsson, Tomas Hoffmann, Michael Deal, Melody E. Grubbs, Jing Li, Blanka Magyari-Kope, Bruce M. Clemens, and Yoshio Nishi, "Theory and experiments of the impact of work-function variability on threshold voltage variability in MOS devices," *IEEE Transactions on Electron Devices*, **59**, (11), 3124–3126, 2012.

[J10] Jing Li and Chung Lam, "Phase change memory (**invited**)," *Science China Information Sciences*, **54**, (5), 1061–1072, 2011.

[J11] Yiran Chen, Hai Li, Cheng-Kok Koh, Guangyu Sun, Jing Li, Yuan Xie, and Kaushik Roy, "Variable-latency adder (VL-Adder) designs for low power and NBTI tolerance," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **18**, (11), 1621–1624, 2010.

[J12] Jing Li, Patrick Ndai, Ashish Goel, Sayeef Salahuddin, and Kaushik Roy, "Design paradigm for robust spin-torque transfer magnetic RAM (STT MRAM) from circuit/architecture perspective (**best paper**)," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **18**, (12), 1710–1723, 2010.

[J13] Jing Li, Kunhyuk Kang, and Kaushik Roy, "Variation estimation and compensation technique in scaled LTPS TFT circuits for low-power low-cost applications," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **28**, (1), 46–59, 2009.

[J14] Jing Li, Aditya Bansal, Swarop Ghosh, and Kaushik Roy, "An alternate design paradigm for low-power, low-cost, testable hybrid systems using scaled LTPS TFTs (**invited**)," *J. Emerg. Technol. Comput. Syst.*, **4**, (3), 13:1–13:19, 2008.

[J15] Jing Li, Aditya Bansal, and Kaushik Roy, "Poly-Si thin-film transistors: An efficient and low-cost option for digital operation," *IEEE Transactions on Electron Devices*, **54**, (11), 2918–2929, 2007.

Referred Conference Papers

[C1] Qing Luo, Jie Yu, Xumeng Zhang, Kan-Hao Xue, Yan Cheng, Tiancheng Gong, Hangbing Lv, Xiaoxin Xu, Peng Yuan, Jiahao Yin, Lu Tai, Shibing Long, Qi Liu, Jing Li, and Ming Liu, "$Nb_{1-x}o_2$ based universal selector with ultra-high endurance (>10^{12}), high speed (10ns) and excellent v_{th} stability," in *2019 IEEE Symposium on VLSI Technology*, Jun. 2019, forthcoming.

[C2] Yue Zha[S], Etienne Nowak, and Jing Li, "Liquid Silicon: A nonvolatile fully programmable processing-in-memory processor with monolithically integrated ReRAM for Big Data/Machine Learning applications," in *2019 IEEE Symposium on VLSI Circuits*, Jun. 2019, forthcoming.

[C3] Jialiang Zhang[S], Yang Liu[S], Gaurav Jain, Yue Zha[S], Jonathan Ta[S], and Jing Li, "MEG: A RISCV-based system simulation infrastructure for exploring memory optimization using FPGAs and Hybrid Memory Cube (**Best Paper Nominee**)," in *2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (**FCCM**)*, Apr. 2019.

[C4] Jialiang Zhang[S] and Jing Li, "PQ-CNN: Accelerating product quantized convolutional neural network (poster)," in *the 2019 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, ser. **FPGA** '19, Feb. 2019.

[C5] Jialiang Zhang[S], Soroosh Khoram[S], and Jing Li, "Efficient large-scale approximate nearest neighbor search on the OpenCL-FPGA," in *Conference on Computer Vision and Pattern Recognition (**CVPR**)*, (Acceptance Rate: 29%, 979 out of over 3300), Jun. 2018.

[C6] Soroosh Khoram[S] and Jing Li, "Adaptive quantization of neural networks," in *International Conference on Learning Representations (**ICLR**)*, Apr. 2018.

[C7] Jialiang Zhang[S] and Jing Li, "PQ-CNN: Accelerating product quantized convolutional neural network (poster)," in *2018 IEEE 26th Annual International Symposium on Field-Programmable Custom Computing Machines (**FCCM**)*, Apr. 2018.

[C8] Jing Li, "Nonvolatile memory outlook: Technology driven or application driven? (**invited**)," in *2018 China Semiconductor Technology International Conference (CSTIC)*, Mar. 12, 2018, pp.1–4.

[C9] Yue Zha[S] and Jing Li, "Liquid Silicon-Monona: A reconfigurable memory-oriented computing fabric with scalable multi-context support," in *23nd International Conference on Architectural Support for Programming Languages and Operating Systems*, ser. **ASPLOS** '18, (Acceptance Rate: 18.2%, 56 out of 307), ACM, Mar. 2018.

[C10] Soroosh Khoram[S], Jialiang Zhang[S], and Jing Li, "Accelerating graph analytics by co-optimizing storage and access on an FPGA-HMC platform," in *Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, ser. **FPGA** '18, (Acceptance Rate*: 24%), New York, NY, USA: ACM, Feb. 2018.

[C11] Jialiang Zhang[S] and Jing Li, "Degree-aware hybrid graph traversal on FPGA-HMC platform," in *Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, ser. **FPGA** '18, (Acceptance Rate*: 24%), Monterey, California, USA: ACM, Feb. 2018.

[C12] Yue Zha[S] and Jing Li, "Liquid Silicon: A data-centric reconfigurable architecture enabled by RRAM technology," in *Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, ser. **FPGA** '18, (Acceptance Rate*: 24%, Ranked **#1** among 100+ submissions), Monterey, California, USA: ACM, Feb. 2018.

[C13] Yue Zha[S] and Jing Li, "RRAM-based reconfigurable in-memory computing architecture with hybrid routing (poster)," in *the 54th Annual Design Automation Conference Work-in-Progress*, ser. DAC-WIP '17, Austin, TX, USA, 2017.

[C14] Yue Zha[S] and Jing Li, "RRAM-based reconfigurable in-memory computing architecture with hybrid routing," in *2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, ser. **ICCAD** '17, (Acceptance Rate: 26%, 105 out of 399), Nov. 2017, pp.527–532.

[C15] Soroosh Khoram[S], Jialiang Zhang[S], Maxwell Strange[S], and Jing Li, "Accelerating large-scale graph analytics with FPGA and HMC (poster)," in *2017 IEEE 25th Annual International Symposium on Field-Programmable Custom Computing Machines (**FCCM**)*, Apr. 2017, pp.82–82.

[C16] Soroosh Khoram[S], Yue Zha[S], Jialiang Zhang[S], and Jing Li, "Challenges and opportunities: From near-memory computing to in-memory computing (**invited**)," in *Proceedings of the 2017 ACM on International Symposium on Physical Design*, ser. **ISPD** '17, Portland, Oregon, USA: ACM, Mar. 2017, pp.43–46.

[C17] Yue Zha[S], Zhiqiang Wei, and Jing Li, "Recent progress in RRAM technology: From compact models to applications (**invited**)," in *2017 China Semiconductor Technology International Conference (CSTIC)*, Mar. 12, 2017, pp.1–4.

[C18] Jialiang Zhang[S], Soroosh Khoram[S], and Jing Li, "Boosting the performance of FPGA-based graph processor using Hybrid Memory Cube: A case for breadth first search," in *Proceedings of the 2017 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, ser. **FPGA** '17, (Acceptance Rate: 25%, 25 out of 101), Monterey, California, USA: ACM, Feb. 2017, pp.207–216.

[C19] Jialiang Zhang[S] and Jing Li, "Improving the performance of OpenCL-based FPGA accelerator for convolutional neural network," in *Proceedings of the 2017 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, ser. **FPGA** '17, (Acceptance Rate: 25%, 25 out of 101), Monterey, California, USA: ACM, Feb. 2017, pp.25–34.

[C20] Yue Zha[S], Jialiang Zhang[S], Zhiqiang Wei, and Jing Li, "A mixed-signal data-centric reconfigurable architecture enabled by RRAM technology (poster)," in *Proceedings of the 2017 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, ser. **FPGA** '17, Monterey, California, USA: ACM, Feb. 2017, pp.285–285.

[C21] Yue Zha[S] and Jing Li, "Reconfigurable in-memory computing with resistive memory crossbar," in *Proceedings of the 35th International Conference on Computer-Aided Design*, ser. **ICCAD** '16, (Acceptance Rate: 24%, 97 out of 408), ACM, Nov. 7, 2016, pp.120.

[C22] Xiaoxin Xu, Q. Luo, Tiancheng Gong, Hangbing Lv, Shibing Long, Qi Liu, S. S. Chung, Jing Li, and Ming Liu, "Fully CMOS compatible 3D vertical RRAM with self-aligned self-selective cell enabling sub-5nm scaling," in *2016 IEEE Symposium on VLSI Technology*, Jun. 2016, pp.1–2.

[C23] Bochen Guan[S] and Jing Li, "A compact model for RRAM including random telegraph noise," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2016, pp.MY-5-1–MY-5-4.

[C24] Jing Li, "Enabling phase-change memory for data-centric computing: Technology, circuitand system (**invited**)," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp.21–24.

[C25] Q. Luo, X. Xu, H. Liu, H. Lv, T. Gong, S. Long, Q. Liu, H. Sun, W. Banerjee, L. Li, J. Gao, N. Lu, S. S. Chung, Jing Li, and M. Liu, "Demonstration of 3d vertical RRAM with ultra low-leakage, high-selectivity and self-

compliance memory cells," in *2015 IEEE International Electron Devices Meeting (**IEDM**)*, 2015, pp.10.2.1–10.2.4.

[C26] Jing Li, Robert Montoye, Masatoshi Ishii, Kevin Stawiasz, Takeshi Nishida, Kim Maloney, Gary Ditlow, Scott Lewis, Tom Maffitt, Richard Jordan, *et al.*, "1Mb 0.41 μm^2 2T-2R cell nonvolatile TCAM with two-bit encoding and clocked self-referenced sensing (**Highlight Paper of the Year**)," in *2013 Symposium on VLSI Circuits*, (Acceptance Rate: 27%, 109 out of 396), 2013, pp.C104–C105.

[C27] P. Y. Du, J. Y. Wu, T. H. Hsu, M. H. Lee, T. Y. Wang, H. Y. Cheng, E. K. Lai, S. C. Lai, H. L. Lung, S. Kim, M. J. BrightSky, Y. Zhu, S. Mittal, R. Cheek, S. Raoux, E. A. Joseph, A. Schrott, Jing Li, and C. Lam, "The impact of melting during reset operation on the reliability of phase change memory," in *2012 IEEE International Reliability Physics Symposium (**IRPS**)*, 2012, pp.6C.2.1–6C.2.6.

[C28] S. Kim, P. Y. Du, Jing Li, M. Breitwisch, Y. Zhu, S. Mittal, R. Cheek, T. H. Hsu, M. H. Lee, A. Schrott, S. Raoux, H. Y. Cheng, S. C. Lai, J. Y. Wu, T. Y. Wang, E. A. Joseph, E. K. Lai, A. Ray, H. L. Lung, and C. Lam, "Optimization of programming current on endurance of phase change memory," in *Proceedings of Technical Program of 2012 VLSI Technology, System and Application (**VLSI-TSA**)*, 2012, pp.1–2.

[C29] Jing Li, Binquan Luan, and Chung Lam, "Resistance drift in phase change memory (**invited**)," in *2012 IEEE International Reliability Physics Symposium (**IRPS**)*, 2012, pp.6C.1.1–6C.1.6.

[C30] Justin Meza, Jing Li, and Onur Mutlu, "A case for small row buffers in non-volatile main memories," in *2012 IEEE 30th International Conference on Computer Design (**ICCD**)*, (Acceptance rate: 25%, 61 out of 241), 2012, pp.484–485.

[C31] Jing Li, Binquan Luan, T. H. Hsu, Y. Zhu, G. Martyna, D. Newns, H. Y. Cheng, S. Raoux, H. L. Lung, and C. Lam, "Explore physical origins of resistance drift in phase change memory and its implication for drift-insensitive materials," in *2011 International Electron Devices Meeting (**IEDM**)*, 2011, pp.12.5.1–12.5.4.

[C32] Jing Li, C. I. Wu, S. C. Lewis, J. Morrish, T. Y. Wang, R. Jordan, T. Maffitt, M. Breitwisch, A. Schrott, R. Cheek, H. L. Lung, and C. Lam, "A novel reconfigurable sensing scheme for variable level storage in phase change memory," in *2011 3rd IEEE International Memory Workshop (**IMW**)*, 2011, pp.1–4.

[C33] B. Rajendran, R. W. Cheek, L. A. Lastras, M. M. Franceschini, M. J. Breitwisch, A. G. Schrott, Jing Li, R. K. Montoye, L. Chang, and C. Lam, "Demonstration of CAM and TCAM using phase change devices," in *2011 3rd IEEE International Memory Workshop (**IMW**)*, 2011, pp.1–4.

[C34] Simone Raoux, Huai-Yu Cheng, Jury Sandrini, Jing Li, and Jean Jordan-Sweet, "Materials engineering for phase change random access memory," in *2011 11th Annual Non-Volatile Memory Technology Symposium Proceeding (NVMTS)*, 2011, pp.1–5.

[C35] C. Y. Wen, Jing Li, S. Kim, M. Breitwisch, C. Lam, J. Paramesh, and L. T. Pileggi, "A non-volatile look-up table design using PCM (phase-change memory) cells," in *2011 Symposium on VLSI Circuits - Digest of Technical Papers*, (Acceptance Rate: 28%, 115 out of 409), 2011, pp.302–303.

[C36] Cheng-Yuan Wen, Jeyanandh Paramesh, Larry Pileggi, Jing Li, SangBum Kim, Jonathan Proesel, and Chung Lam, "Post-silicon calibration of analog CMOS using phase-change memory cells," in *2011 Proceedings of the ESSCIRC (**ESSCIRC**)*, 2011, pp.423–426.

[C37] J. Y. Wu, M. Breitwisch, S. Kim, T. H. Hsu, R. Cheek, P. Y. Du, Jing Li, E. K. Lai, Y. Zhu, T. Y. Wang, H. Y. Cheng, A. Schrott, E. A. Joseph, R. Dasaka, S. Raoux, M. H. Lee, H. L. Lung, and C. Lam, "A low power phase change memory using thermally confined TaN/TiN bottom electrode," in *2011 International Electron Devices Meeting (**IEDM**)*, 2011, pp.3.2.1–3.2.4.

[C38] Jing Li, Patrick Ndai, Goel Ashish, and Kaushik Roy, "Variation resilient spin torque transfer MRAM (poster)," in *GSRC Workshop*, Dallas, TX, USA, 2009.

[C39] Jing Li, Patrick Ndai, Ashish Goel, Haixin Liu, and Kaushik Roy, "An alternate design paradigm for robust spin-torque transfer magnetic RAM (STT MRAM) from circuit/architecture perspective," in *Proceedings of the 2009 Asia and South Pacific Design Automation Conference*, ser. **ASP-DAC** '09, Yokohama, Japan: IEEE Press, 2009, pp.841–846.

[C40] Jing Li and Kaushik Roy, "Robust heterogeneous system design in spintronics: Error resilient spin torque MRAM (STT MRAM) design," in *the 46th Annual Design Automation Conference PHD Forum*, ser. **DAC** '09, (Acceptance Rate: 22%, 148 out of 684), 2009.

[C41] Xiao Zhang, Jing Li, M. Grubbs, M. Deal, B. Magyari-Köpe, B. M. Clemens, and Y. Nishi, "Physical model of the impact of metal grain work function variability on emerging dual metal gate MOSFETs and its implication for SRAM reliability," in *2009 IEEE International Electron Devices Meeting (**IEDM**)*, 2009, pp.1–4.

[C42] Jing Li, Charles Augustine, Sayeef Salahuddin, and Kaushik Roy, "Modeling of failure probability and statistical design of spin-torque transfer magnetic random access memory (STT MRAM) array for yield enhancement," in *2008 45th ACM/IEEE Design Automation Conference (**DAC**)*, (Acceptance Rate: 23%, 147 out of 639), 2008, pp.278–283.

[C43] Jing Li, Haixin Liu, S. Salahuddin, and Kaushik Roy, "Variation-tolerant spin-torque transfer (STT) MRAM array for yield enhancement," in *2008 IEEE Custom Integrated Circuits Conference (**CICC**)*, 2008, pp.193–196.

[C44] Jing Li and Kaushik Roy, "Modeling of failure probability and statistical design of spin-torque transfer magnetic RAM (STT MRAM) array for yield enhancement," in *SRC Technology and Talent for the 21st Century Technology (TECHCON)*, 2008.

[C45] Yiran Chen, Hai Li, Jing Li, and Cheng-Kok Koh, "Variable-latency adder (VL-adder): New arithmetic circuit design practice to overcome NBTI," in *2007 ACM/IEEE International Symposium on Low Power Electronics and Design (**ISLPED**)*, 2007, pp.195–200.

[C46] Jing Li, S. Ghosh, and Kaushik Roy, "A generic and reconfigurable test paradigm using low-cost integrated Poly-Si TFTs," in *2007 IEEE International Test Conference (**ITC**)*, 2007, pp.1–10.

[C47] Jing Li, Kunhyuk Kang, Aditya Bansal, and Kaushik Roy, "High performance and low power electronics on flexible substrate," in *2007 44th ACM/IEEE Design Automation Conference (**DAC**)*, (Acceptance Rate*: 13%), 2007, pp.274–275.

[C48] Jing Li, Kunhyuk Kang, and Kaushik Roy, "Novel variation-aware circuit design of scaled LTPS TFT for ultra low power, low-cost applications," in *2007 IEEE International Conference on Integrated Circuit Design and Technology (**ICICDT**)*, 2007, pp.1–4.

[C49] Jing Li and Kaushik Roy, "Low power and variation tolerant digital circuit design in sub-micron regime using low cost LTPS TFTs," in *SRC Technology and Talent for the 21st Century Technology (TECHCON)*, 2007.

[C50] Jing Li, Aditya Bansal, and Kaushik Roy, "Exploring low temperature Poly-Si for low cost and low power submicron digital operation," in *2006 64th Device Research Conference (**DRC**)*, 2006, pp.61–62.

Issued Patents

[P1] Jing Li, *Nonvolatile range-checking content addressable memory*, US Patent 9,711,221, 2016.

[P2] Jing Li, *Computer architecture using compute/storage tiles*, US Patent 9,779,785, 2015.

[P3] Jing Li, *High density content addressable memory*, US Patent 9,979,649 B2, 2015.

[P4] Bing Dai, Chung H Lam, and Jing Li, *Adaptive reference tuning for endurance enhancement of non-volatile memories*, US Patent 9,122,404, 2013.

[P5] Bing Dai, Chung H Lam, and Jing Li, *Adaptive reference tuning for endurance enhancement of non-volatile memories*, US Patent 9,250,816, 2013.

[P6] Chung H Lam and Jing Li, *Self-aligned patterning technique for semiconductor device features*, US Patent 8,927,424, 2013.

[P7] Chung H Lam and Jing Li, *Self-aligned patterning technique for semiconductor device features*, US Patent 8,927,425, 2013.

[P8] Chung H Lam and Jing Li, *Single mask spacer technique for semiconductor device features*, US Patent 8,658,498, 2013.

[P9] Chung H Lam and Jing Li, *Single-mask spacer technique for semiconductor device features*, US Patent 8,652,901, 2013.

[P10] Chung H Lam and Jing Li, *Vertical surround gate formation compatible with cmos integration*, US Patent 8,815,718, 2013.

[P11] Chung H Lam, Jing Li, and Edward W Kiewra, *Electrical coupling of memory cell access devices to a word line*, US Patent 9,343,545, 2013.

[P12] Chung H Lam, Jing Li, and Edward W Kiewra, *Electrical coupling of memory cell access devices to a word line*, US Patent 9,299,804, 2013.

[P13] Jing Li and Dinesh C Verma, *Self-adjusting phase change memory storage module*, US Patent 9,563,371, 2013.

[P14] Matthew J BrightSky, Chung H Lam, Jing Li, Alejandro G Schrott, and Norma E Sosa Cortes, *Phase change memory cell with large electrode contact area*, US Patent 8,921,820, 2012.

[P15] Matthew J BrightSky, Chung H Lam, Jing Li, Alejandro G Schrott, and Norma E Sosa Cortes, *Phase change memory cell with large electrode contact area*, US Patent 8,946,073, 2012.

[P16] Matthew J BrightSky, Chung H Lam, Jing Li, Alejandro G Schrott, and Norma E Sosa Cortes, *Phase change memory cell with large electrode contact area*, US Patent 9,166,161, 2012.

[P17] Leland Chang, Chung H Lam, Jing Li, and Robert K Montoye, *Sense scheme for phase change material content addressable memory*, US Patent 8,687,398, 2012.

[P18] Bing Dai, Chung H Lam, and Jing Li, *Memory controller for memory with mixed cell array and method of controlling the memory*, US Patent 9,606,908, 2012.

[P19] Bing Dai, Chung H Lam, and Jing Li, *Memory controller for memory with mixed cell array and method of controlling the memory*, US Patent 9,032,136, 2012.

[P20] Bing Dai, Chung H Lam, and Jing Li, *Memory with mixed cell array and system including the memory*, US Patent 9,298,383, 2012.

[P21] Bing Dai, Chung H Lam, and Jing Li, *Memory with mixed cell array and system including the memory*, US Patent 9,146,852, 2012.

[P22] Bing Dai, Chung H Lam, and Jing Li, *Memory with mixed cell array and system including the memory*, US Patent 9,311,009, 2012.

[P23] John K DeBrosse, Kailash Gopalakrishnan, Chung H Lam, and Jing Li, *Decoding scheme for bipolar-based diode three-dimensional memory requiring bipolar programming*, US Patent 8,755,213, 2012.

[P24] Kailash Gopalakrishnan, Chung H Lam, Jing Li, and Robert K Montoye, *Decoding scheme for bipolar-based diode three-dimensional memory requiring unipolar programming*, US Patent 8,842,491, 2012.

[P25] Kailash Gopalakrishnan, Chung H Lam, Jing Li, and Robert K Montoye, *Decoding scheme for bipolar-based diode three-dimensional memory requiring unipolar programming*, US Patent 8,902,690, 2012.

[P26] Chung H Lam, Jing Li, and Kailash Gopalakrishnan, *3d architecture for bipolar memory using bipolar access device*, US Patent 8,873,271, 2012.

[P27] Chung H Lam, Jing Li, Binquan Luan, Glenn J Martyna, and Dennis M Newns, *Drift-insensitive or invariant material for phase change memory*, US Patent 8,737,121, 2012.

[P28] Chung H Lam, Jing Li, Binquan Luan, Glenn J Martyna, and Dennis M Newns, *Drift-insensitive or invariant material for phase change memory*, US Patent 8,767,447, 2012.

[P29] Chung H Lam, Jing Li, and Robert K Montoye, *Multi-bit resistance measurement*, US Patent 8,638,598, 2012.

[P30] Chung H Lam, Jing Li, and Robert K Montoye, *Multi-bit resistance measurement*, US Patent 8,837,198, 2012.

[P31] Chung H Lam, Jing Li, and Robert K Montoye, *Writing scheme for phase change material-content addressable memory*, US Patent 8,560,902, 2012.

[P32] Chung H Lam, Jing Li, and Robert K Montoye, *Writing scheme for phase change material-content addressable memory*, US Patent 8,943,374, 2012.

[P33] Chung H Lam and Jing Li, *Drift mitigation for multi-bits phase change memory*, US Patent 8,854,872, 2011.

[P34] Chung H Lam and Jing Li, *Drift mitigation for multi-bits phase change memory*, US Patent 9,269,435, 2011.

[P35] Chung H Lam and Jing Li, *Energy-efficient row driver for programming phase change memory*, US Patent 8,614,911, 2011.

[P36] Chung H Lam and Jing Li, *Parallel programming scheme in multi-bit phase change memory*, US Patent 8,605,497, 2011.

[P37] Chung Hon Lam, Jing Li, and Robert Montoye, *Content addressable memories with wireline compensation*, US Patent 8,446,748, 2011.

[P38] Chung H Lam, Scott C Lewis, and Jing Li, *Reconfigurable multi-level sensing scheme for semiconductor memories*, US Patent 8,717,802, 2010.

Pending Patents

[PP1] Jing Li and Jialiang Zhang, *Computer architecture for high-speed graph traversal*, Filed by the Wisconsin Alumni Research Foundation (WARF), 2018.

[PP2] Jing Li and Jialiang Zhang, *Neural network processor with on-chip convolution kernel storage*, Filed by the Wisconsin Alumni Research Foundation (WARF), 2018.

[PP3] Soroosh Khoram and Jing Li, *Associative computer providing semi-parallel architecture*, Filed by the Wisconsin Alumni Research Foundation (WARF), 2016.

[PP4] Jing Li and Jialiang Zhang, *High-speed graph processor*, Filed by the Wisconsin Alumni Research Foundation (WARF), 2016.

[PP5] Jing Li and Jialiang Zhang, *Matrix processor with localized memory*, Filed by the Wisconsin Alumni Research Foundation (WARF), 2016.

[PP6] Chung H Lam and Jing Li, *Self-aligned approach for drain diffusion in field effect transistors*, US Patent US20140264557A1, 2013.

Non-referred Technical Reports

[R1] Justin Meza, Jing Li, and Onur Mutlu, "Evaluating row buffer locality in future non-volatile main memories," Carnegie Mellon University (CMU), Tech. Rep. 2012-002, 2012, SAFARI Technical Report.

[R2] Jing Li, "Body history study on 12S eDRAM sensing operation," Semiconductor Research and Development Center (SRDC), IBM, Fishkill, Tech. Rep., 2008.

Major Invited Talks

- "Liquid Silicon: A New Computing Paradigm Enabled by Monolithic 3D Cross-point Memory," Dept. of Electrical and Computer Engineering, **Cornell University**, Dec. 12th, 2018.
- "Liquid Silicon: A New Computing Paradigm Enabled by Monolithic 3D Cross-point Memory," Dept. of Electrical and Computer Engineering, **Carnegie Mellon University (CMU)**, Nov. 30th, 2018.
- "Liquid Silicon: A New Computing Paradigm Enabled by Monolithic 3D Cross-point Memory," Dept. of Computer Science, **University of Chicago**, Nov. 6th, 2018.
- "Liquid Silicon: A New Computing Paradigm Enabled by Monolithic 3D Cross-point Memory," Dept. of Electrical Engineering, **Yale University**, Nov. 2nd, 2018.
- "Liquid Silicon: A New Computing Paradigm Enabled by Monolithic 3D Cross-point Memory," Dept. of Electrical and Computer Engineering, University of California, Los Angeles (**UCLA**), 12:30pm–1:30pm PST, Oct. 15th, 2018.
- "Liquid Silicon: A New Computing Paradigm Enabled by Monolithic 3D Cross-point Memory," **Harvard University**, 3:00pm–4:00pm EST, September 28th, 2018.
- "Enabling Nonvolatile Memory for Data-Centric Computing: Technology, Circuit and System," **Panasonic Corp.**, 4:00pm–5:00pm, Kyoto, Japan, July 16th, 2015.
- "Enabling Phase-change Memory for Data-Centric Computing: Technology, Circuit and System," Special session at IEEE international Symposium on Circuits and Systems (**ISCAS**), Lisbon, May 25th, 2015.
- "Emerging-Materials-Enabled Devices for Data-Centric Computing," Special guest lecture co-sponsored by CTO, APTD, and WPDN, **Applied Materials**, 3:00pm–4:00pm PST, August 27th, 2014.
- "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Colloquium of Electrical and Computer Engineering department at **Purdue University**, 3:00pm–4:00pm EST, April 28th, 2014
- "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Colloquium of Electrical and Systems department at **University of Pennsylvania**, 11:00am–12:00pm EST, March 17th, 2014

- "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Electrical Engineering Seminar Series at **Harvard University**, 3:00pm–4:00pm EST, March 7th, 2014
- "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Electrical and Computer Engineering Department Seminar at University of Illinois Urbana-Champaign (**UIUC**), 4:00pm–5:00pm CST, March 3rd, 2014
- "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Computer Engineering Seminar at University of California Santa Barbara (**UCSB**), 11:00am–12:00pm PST, February 12th, 2014
- "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Joint CSSI and CALCM Seminar Series at Carnegie Mellon University (**CMU**), 12:00pm–1:00pm EST, Nov. 1st, 2013
- "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Electrical Engineering Seminar Series at University of California, Los Angeles (**UCLA**), 1:00pm–2:30pm PDT, Oct 28th, 2013
- "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Electrical Engineering Seminar Series at **Princeton University**, 12:30pm–1:30pm EST, Oct 16th, 2013
- "A Holistic View of Architecting Storage Class Memory into Future System," Invited tutorial on system-technology interaction, International Memory Workshop (**IMW**), Milan, Italy, May 20, 2012
- "Resistance Drift in Phase Change Memory," The IEEE International Reliability Physics Symposium (**IRPS**), Anaheim, CA, April 19, 2012
- "Phase Change Memory," The Connecticut Microelectronics and Optoelectronics Consortium (**CMOC**) Twenty-First Annual Symposium, Storrs, CT, April 11, 2012
- "Phase Change Memory Design: Challenges and Opportunities," China Semiconductor Technology International Conference (**SEMICON** China), Shanghai, China, March 15-17, 2011
- "Design Challenges in Multi-Level Phase Change Memory," New Non-Volatile Memory Workshop (NNVMW'10), Industrial Technology Research Institute (**ITRI**), Hsin-chu, Taiwan Nov. 11, 2010
- "Robust Design in Emerging Technologies," **Intel Corporation**, CA, 2:00 pm-3:30 pm PDT, Feb.1,2008
- "A Genetic and Reconfigurable Test Paradigm Using Low-Cost Integrated Poly-Si TFT," **LSI Corporation**, CA, 1:30 pm-3:30 pm PDT, Oct.19, 2007

Professional Activity (External)

Editor	Journal of Low Power Electronics (**JOLPE**), 2017–
Area Chair	IEEE Conference on Artificial Intelligence Circuits and Systems (**AICAS**), 2018–
Publicity Chair	International Symposium on Field-Programmable Gate Arrays (**FPGA**), 2018–2019
Publicity Chair	International Symposium on Low Power Electronics and Design (**ISLPED**), 2017–2018
Organizing committee	International Memory Workshop (**IMW**), 2013–
Publicity Chair	International Memory Workshop (**IMW**), 2016–2017
General Chair	International Memory Workshop (**IMW**), 2015–2016
Technical Chair	International Memory Workshop (**IMW**), 2014–2015
Finance Chair	International Memory Workshop (**IMW**), 2013–2014
Organizer & Chair	Special session at International Symposium on Circuits and Systems (**ISCAS**), 2016
Organizer & Chair	Short course on RRAM at International Memory Workshop (**IMW**), 2013
Program committee	International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), 2019– International Symposium on Computer Architecture (**ISCA**), 2019– **SysML**, 2019– ACM SIGDA Technical Committee on FPGAs and Reconfigurable Computing (**TC-FPGA**), 2018– International Symposium on Field-Programmable Gate Arrays (**FPGA**), 2017– International Symp. on Field-Programmable Custom Computing Machines (**FCCM**), 2017– Design Automation Conference (**DAC**), 2012–2014, 2017– International Conference on Computer-Aided Design (**ICCAD**), 2015– Great Lakes Symposium on VLSI (**GLSVLSI**), 2017– International Symposium on Low Power Electronics and Design (**ISLPED**), 2017– International Symposium on Circuits and Systems (**ISCAS**), 2016– International Memory Workshop (**IMW**), 2013– International Symposium on Microarchitecture (**MICRO**, external), 2016 International Electron Devices Meeting (**IEDM**), 2016
Reviewer	IEEE Transaction on Computers (**TC**), 2018– IEEE Micro, 2018– International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication (**EIPBN**), 2018– IEEE Journal of Solid-State Circuits (**JSSC**), 2010, 2017– IEEE Transactions on VLSI Systems (**TVLSI**), 2015, 2017– IEEE Transactions on Electron Devices (**TED**), 2010, 2016– Journal of Low Power Electronics (**JOLPE**), 2017– IEEE Transactions on Neural Networks and Learning Systems (**TNNLS**), 2017– Journal of Electronic Testing (**JETTA**, 2015) Journal on Emerging and Selected Topics in Circuits and Systems (**JETCAS**), 2015 IEEE Transactions on Circuits and Systems-Part I (**TCAS-I**), 2015 IEEE Electron Device Letters (**EDL**), 2010, 2011 IEEE International Symposium on Information Theory (**ISIT**), 2010 IEEE Device Research Conference (**DRC**), 2010
Panelist	DOE, 2018– NSF, 2014–
Member	JEDEC Memory Standard, 2011–
Member	Society of Women Engineers (SWE), 2006–
Member	Computing Research Association for Women (CRA-W), 2012–
μMBA	Perspective business/technical leaders at IBM, 2011