Jing (Jane) Li

SELECTED HONORS

- ***DARPA Young Faculty Award***, Defense Advanced Research Projects Agency, 2016
- *WARF Innovation Awards (WIA) Finalist,* University of Wisconsin-Madison (6 out of 400++ patents), 2016
- *VLSI Transactions* ***Best Paper Award****,* IEEE Circuits and Systems Society, 2013
- *Outstanding Research Division Technical Achievement Award* (**A-level, for successfully achieving CEO milestone on Storage Class Memory**), IBM T. J. Watson, 2012
- *IBM High Value Patent Application Awards,* IBM T. J. Watson, 2014
- *IBM Invention Achievement Awards,* IBM T. J. Watson, 2010-15
- *IBM PhD Fellowship Award*, 2008-09
- *The Dean's and Semester Honors for Outstanding Scholastics Performance*, Purdue University, 2007-08.
- *Magoon Award* for Excellence in Teaching, Purdue University, 2005-06
- *Meissner Fellowship Award*, Electrical and Computer Engineering department, Purdue University, 2004-05.

PUBLICATIONS

Journal Papers

1. **Jing Li**, R. Montoye, M. Ishii, L. Chang, "1Mb 0.41 μm^2 2T-2R Cell Nonvolatile TCAM with Two-bit Encoding and Clocked Self-Referenced Sensing," *Vol. 49 , Issue 4, pp. 896 – 907, IEEE Journal of Solid-State Circuits (JSSC)* (**INVITED**), April, 2014
2. K. Cil, Y. Zhu, **Jing Li**, C. H. Lam and H. Silva, "Assisted cubic to hexagonal phase transition in GeSbTe thin films on underlying silicon nitride," *Thin Solid Films*, vol. 536, pp. 216-219, 2013
3. X. Zhang, J. Mitard, L-A Ragnarsson, T. Hoffmann, M. Deal, M. Grubbs, **Jing Li**, B. Magyari-Kope, B. Clemens, Yoshio Nishi, "Theory and Experiments of the Impact of Work Function Variability on Threshold Voltage Variability in MOS Devices," *IEEE Transactions on Electron Devices (TED)*, vol.59, no.11, pp. 3124 – 3126, 2012
4. A. Cywar, **Jing Li**, C. Lam, H. Silva, "The impact of heater-recess and load matching in phase change memory mushroom cells," Nanotechnology 23, 22, 225201(2012).
5. **Jing Li** and Chung Lam, "Phase Change Memory," *Science China (Information Sciences)* (**INVITED**), Vol 54, NO. 5: 1061-1072 (2011).
6. **Jing Li**, P. Ndai, A.Goel, S. Salahuddin, and Kaushik Roy, "Design Paradigm for Robust Spin-Torque Transfer Magnetic RAM (STT MRAM) from Circuit/Architecture Perspective," *IEEE Transaction on VLSI Systems (TVLSI),* vol. 18, issue 12, pp.1710-1723, Dec., 2010 (**IEEE Circuits and Systems Society VLSI Transactions Best Paper Award, 2013)**
7. Y. Chen, H. Li, C-K Koh, Y. Sun, **Jing Li**, Y. Xie and Kaushik Roy, "Variable-Latency Adder (VL-Adder) Designs for Low Power and NBTI Tolerance," *IEEE Transaction on VLSI Systems (TVLSI),* vol. 18, issue 11, pp.1621-1624, Nov., 2010
8. **Jing Li,** K. Kang and Kaushik Roy; "Variation Estimation and Compensation Technique in Scaled LTPS TFT Circuits for Low Power, Low-Cost Applications," *IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems (TCAD)*, vol. 28, no. 1, pp.46-59, Jan., 2009
9. **Jing Li**, A. Bansal, S. Ghosh, and Kaushik Roy, "An alternate design paradigm for low-power, low-cost, testable hybrid systems using scaled LTPS TFTs," *ACM Journal on Emerging Technologies in Computing Systems*(**INVITED**), vol. 4, issue 3, pp13.1-13.19, Aug., 2008
10. **Jing Li**, A. Bansal and Kaushik Roy; "Poly-Si Thin Film Transistors: An efficient and low cost option for digital sub-threshold operation," *IEEE Transactions on Electron Devices (TED),* vol. 54, no. 11, pp 2918-2929, Nov., 2007 (**the 1st proposal in literature, experimentally verified by Toshiba in 2010**)

Peer-Reviewed Conference Papers

11. Jialiang Zhang, Soroosh Khoram and **Jing Li,** " Boosting the Performance of FPGA-based Graph Processor using Hybrid Memory Cube: A Case for Breadth First Search", accepted by ACM/SIGDA FPGA 2017

12. Yue Zha, Jialiang Zhang and **Jing Li** "Liquid Silicon: A Data-Centric Mixed- Signal Reconfigurable Architecture enabled by RRAM Technology ", accepted by ACM/SIGDA FPGA 2017

13. Yue Zha and **Jing Li**, "Reconfigurable In-Memory Computing with Resistive Memory Crossbar", International Conference on Computer-Aided Design (*ICCAD*), 2016

14. X. Xu, Q. Luo, T. Gong, H. Lv, S. Long, Q. Liu, S. S. Chung, **Jing Li** and M. Liu, "Fully CMOS Compatible 3D Vertical RRAM with Self-aligned Self-selective Cell Enabling Sub-5nm Scaling Capability", *Symp. on VLSI Technology,* 2016

15. Bochen guan and **Jing Li,** "A Compact Model for RRAM Including Random Telegraph Noise", *IEEE International Reliability Physics Symposium (IRPS*), 2015

16. Q. Luo, X. Xu, H. Liu, H. Lv, T. Gong, S. Long, Q. Liu, H. Sun, W. Banerjee, L. Li, J. Gao, N. Lu, S.S. Chung, **Jing Li**, and M. Liu, "Demonstration of 3D Vertical RRAM with Ultra Low-leakage, High-selectivity and Self-compliance Memory Cells", *Intl. Electron Device Meeting (IEDM) Dig. Tech.,* 2015

17. **Jing Li,** "Enabling Phase-Change Memory for Data-Centric Computing: Technology, Circuit and System", (**INVITED**), *IEEE International Symposium on Circuits and Systems (ISCAS),* 2015

18. **Jing Li**, R. Montoye, M. Ishii, K. Stawiasz, T. Nishida, K. Maloney, G. Ditlow, S. Lewis, T. Maffitt, R. Jordan, L. Chang, P. Song, "1Mb 0.41 µm2 2T-2R Cell Nonvolatile TCAM with Two-bit Encoding and Clocked Self-Referenced Sensing, " *Symp. on VLSI Circuits* (**Highlight Paper of the Year**), Kyoto, Japan, 2013

19. Justin Meza, **Jing Li**, Onur Mutlu. "A Case for Small Row Buffers in Non-Volatile Main Memories," Proceedings of the 30th IEEE *International Conference on Computer Design (ICCD),* 2012

20. **Jing Li**, B. Luan and C. Lam, "Resistance Drift in Phase Change Memory" (**INVITED**), *IEEE International Reliability Physics Symposium (IRPS*), 2012

21. P. Y. Du, J. Y. Wu, T. H. Hsu, S. Kim, M. H. Lee, T. Y. Wang, M. Breitwisch, Y. Zhu, S. Mittal, R. Cheek, H. Y. Cheng, S. Raoux, E. A. Joseph, E. K. Lai, S. C. Lai, A. Schrott, **Jing Li,** H. L. Lung and C. Lam, "The Impact of Melting during RESET Operation on the Reliability of Phase Change Memory," *IEEE International Reliability Physics Symposium (IRPS),* 2012

22. S. Raoux, H-Y Chen, J. Sandrini, **Jing Li**, J. Sweet, "Materials Engineering for Phase Change Random Access Memory," *Non-volatile Memory Technology Symposium, (NVMTS*), 2011

23. S. Kim, P-Y Du, **Jing Li,** M. J. Breitwisch, Y. Zhu, S. Mittal, R. Cheek, T-H Hsu, M-H Lee, A. Schrott, S. Raoux, H-Y Cheng, S-C Lai, C-I Wu, T-Y Wang, E. Joseph, E-K Lai, A. RAY, H-L Lung and C Lam, "Optimization of Programming Current on Endurance of Phase Change Memory," *VLSI-TSA*, 2012

24. **Jing Li**, Binquan Luan, T.H. Hsu, Y. Zhu, G. Martyna, D. Newns, H.Y. Cheng, S. Raoux, H. L. Lung and C. Lam, "Explore Physical Origins of Resistance Drift in Phase Change Memory and its Implication for Drift-insensitive Materials, " *Intl. Electron Device Meeting (IEDM) Dig. Tech.,* 2011

25. J.Y. Wu, M. Breitwisch, S. Kim, T.H. Hsu, R. Cheek, P.Y. Du, **Jing Li**, E. K. Lai, Y. Zhu, T.Y. Wang , H.Y. Cheng, A. Schrott, E.A. Joseph, R. Dasaka, S. Raoux, M.H. Lee, H.L. Lung and C. Lam, "A Low Power Phase Change Memory Using Thermally Confined TaN/TiN Bottom Electrode", *Intl. Electron Device Meeting (IEDM) Dig. Tech.,* 2011

26. C.-Y. Wen, **Jing Li**, Jonathan Proesel, S. Kim, C. Lam, J. Paramesh, L. T. Pileggi, "Post-Silicon Calibration of Analog CMOS Using Phase-Change Memory Cells," the 41st European Solid-State Circuits Conference (ESSCIRC), Sep. 12th – 16th , Helsinki, Finland, 2011

27. C.-Y. Wen, **Jing Li**, S. Kim, M. Breitwisch, C. Lam, J. Paramesh, L. T. Pileggi, "A Non-volatile Look-Up Table Design Using PCM (Phase-Change Memory) Cells," *Symp. on VLSI Circuits,* Kyoto, Japan, 2011

28. **Jing Li**, C.I. Wu, S. Levis, J. Morrish, T. Y. Wang, R. Jordan, T. Maffitt, M. Breitwisch, Hsiang-Lan Lung, C. Lam, "A Novel Reconfigurable Sensing Scheme for Variable Level Storage in Phase Change Memory," *International Memory Workshop (IMW),* May 22nd – 25th, 2011, Monterey, California, USA, 2011

29. B. Rajendran, R. Cheek, L. Lastras, M. Franceschini, M. Breitwisch, A. Schrott, **Jing Li**, R. Montoye, L. Chang and C. Lam, "Demonstration of CAM and TCAM using Phase Change Devices," *International Memory Workshop (IMW),* May 22nd – 25th, 2011, Monterey, California, USA, 2011

30. X. Zhang, **Jing Li**, M. Grubbs, M. Deal, B. Magyari-Kope, B. Clemens and Yoshio Nishi, "Physical Model of the Impact of Metal Grain Work Function Variability on Emerging Dual Metal Gate MOSFETs and its Implication for SRAM Reliability," *Intl. Electron Device Meeting (IEDM) Dig. Tech.,* 2009

31. **Jing Li** and Kaushik Roy, "Robust Heterogeneous System Design in Spintronics: Error Resilient Spin Torque MRAM (STT MRAM) Design," *PH.D Forum, Design Automation Conf. (DAC),* 2009

32. **Jing Li**, P. Ndai, A.Goel, H. Liu, and Kaushik Roy, "An Alternate Design Paradigm for Robust Spin-Torque Transfer Magnetic RAM (STT MRAM) from Circuit/Architecture Perspective," *Asia and South Pacific Design Automation Conf. (ASP-DAC),* 2009

33. **Jing Li**, Patrick Ndai, goel ashish, Kaushik Roy, "Variation Resilient Spin Torque Transfer MRAM" (Poster), GSRC Workshop, Dallas TX, Mar 9, 2009.

34. **Jing Li** and Kaushik Roy, "Modeling of Failure Probability and Statistical Design of Spin-Torque Transfer Magnetic RAM (STT MRAM) Array for Yield Enhancement," *Technology and Talent for the 21st Century Technology (TECHCON), SRC,* 2008

35. **Jing Li,** H. Liu, S. Salahuddin, and Kaushik Roy, "Variation-Tolerant Spin-Torque Transfer (STT) MRAM Array for Yield Enhancement," Custom Integrated Circuits Conf. *(CICC),* 2008

36. **Jing Li**, C. Augustine, S. Salahuddin, and Kaushik Roy, "Modeling of Failure Probability and Statistical Design of Spin-Torque Transfer Magnetic Random Access Memory (STT MRAM) Array for Yield Enhancement," *Design Automation Conf. (DAC),* 2008

37. **Jing Li**, S. Ghosh, and Kaushik Roy, "A generic and reconfigurable test paradigm using low-cost integrated Polysilicon TFTs," *Intl. Test Conf. (ITC)*, 2007

38. Y. Chen, H. Li, **Jing Li** and Cheng-Kok Koh, "Variable-latency Adder (VL-Adder): New Arithmetic Circuit Design Practice to Overcome NBTI," *Intl. Symp. on Low Power Electronic Design (ISLPED)*, 2007

39. **Jing Li** and Kaushik Roy, "Low Power and Variation Tolerant Digital Circuit Design in Sub-micron Regime using Low Cost LTPS TFTs," *Technology and Talent for the 21st Century Technology (TECHCON), SRC,* 2007

40. **Jing Li,** K. Kang and Kaushik Roy, "Novel variation-aware circuit design of scaled LTPS TFT for ultra low power, low-cost applications," *Intl. Conf. on IC Design & Technology (ICICDT),* 2007

41. **Jing Li**, K. Kang, A. Bansal and Kaushik Roy, "High performance and low power electronics on flexible substrates," *Wild and Crazy Idea session* (acceptance rate ~ **13%**), *Design Automation Conf. (DAC),* 2007

42. **Jing Li**, A. Bansal and Kaushik Roy; "Exploring low temperature Poly-Si for low cost and low power sub-micron digital operation," *Device Research Conf. (DRC)*, 2006

SELECTED INVITED TALKS (EXTERNAL)

1. "Enabling Nonvolatile Memory for Data-Centric Computing: Technology, Circuit and System," **Panasonic Corp**., 4:00pm to 5:00pm, Kyoto, Japan, July 16th, 2015

2. "Enabling Phase-change Memory for Data-Centric Computing: Technology, Circuit and System," Special session at IEEE international Symposium on Circuits and Systems (**ISCAS**), Lisbon, May 25th, 2015

3. "Emerging-Materials-Enabled Devices for Data-Centric Computing," Special guest lecture co-sponsored by CTO, APTD, and WPDN, **Applied Materials**, 3:00pm – 4:00pm PST, August 27th, 2014

4. "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Colloquium of Electrical and Systems department at **Purdue University,** 3:00pm – 4:00pm EST, April 28th, 2014

5. "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Colloquium of Electrical and Systems department at **University of Pennsylvania,** 11:00am – 12:00pm EST, March 17th, 2014

6. "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Electrical Engineering Seminar Series at **Harvard University,** 3:00pm – 4:00pm EST, March 7th, 2014

7. "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Electrical and Computer Engineering Department Seminar at University of Illinois Urbana-Champaign **(UIUC),** 4:00pm – 5:00pm CST, March 3rd, 2014

8. "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Computer Engineering Seminar at **University of California Santa Barbara (UCSB),** 11:00am – 12:00pm PST, February 12th, 2014

9. "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Joint CSSI and CALCM Seminar Series at **Carnegie Mellon University (CMU)**, 12:00pm – 1:00pm EST, Nov. 1st, 2013

10. "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Electrical Engineering Seminar Series at **University of California, Los Angeles (UCLA),** 1:00pm – 2:30pm PDT, Oct 28th, 2013

11. "Data Centric Computing in Emerging Technologies: A PCM-CMOS Hybrid Hardware Accelerator," Electrical Engineering Seminar Series at **Princeton University**, 12:30pm – 1:30pm EST, Oct 16th, 2013

12. "A Holistic View of Architecting Storage Class Memory into Future System," Invited tutorial on system-technology interaction, International Memory Workshop (**IMW**), Milan, Italy, May 20, 2012

13. "Resistance Drift in Phase Change Memory," The IEEE International Reliability Physics Symposium (**IRPS**), Anaheim, CA, April 19, 2012

14. "Phase Change Memory," The Connecticut Microelectronics and Optoelectronics Consortium (**CMOC**) Twenty-First Annual Symposium, Storrs, CT, April 11, 2012

15. "Phase Change Memory Design: Challenges and Opportunities," China Semiconductor Technology International Conference (**SEMICON China)**, Shanghai, China, March 15-17, 2011

16. "Design Challenges in Multi-Level Phase Change Memory," New Non-Volatile Memory Workshop (NNVMW'10), Industrial Technology Research Institute (**ITRI**), Hsin-chu, Taiwan Nov. 11, 2010

17. "Robust Design in Emerging Technologies," **Intel Corporation**, CA, 2:00 pm-3:30 pm PDT, Feb.1,2008

18. "A Genetic and Reconfigurable Test Paradigm Using Low-Cost Integrated Poly-Si TFT," **LSI Corporation**, CA, 1:30 pm-3:30 pm PDT, Oct.19, 2007